METHOD TO FORM SHALLOW TRENCH ISOLATION WITH ROUNDED UPPER CORNER FOR ADVANCED SEMICONDUCTOR CIRCUITS

Background of the Invention

[0001] This invention relates to semiconductor processing, particularly to a shallow-trench-isolation structure and the method of forming a trench with rounded upper corners.

[0002] Modern integrated-circuit technology is capable of packing a large number of individual circuit-elements near the surface of a small silicon chip. The individual elements are connected according to the circuit design by metal lines. The metal lines are imbedded in a matrix of multiple layers of metal and dielectric material. Beneath the silicon-chip surface, the circuit-elements are isolated from each other by regions of silicon dioxide to prevent unwanted electrical current passage between the circuit-elements.

[0003] The silicon dioxide regions may be formed in two techniques well known in the art of semiconductor processing. The Local Oxidation of Silicon (LOCOS) process forms the dioxide regions by thermally oxidizing a portion of the chip surface not designated for active circuit devices; the Shallow Trench Isolation (STI) process forms the dioxide regions by removing silicon from a portion of the chip surface and refilling with silicon-dioxide material where the isolation is required.

[0004] Generally speaking, LOCOS is not suitable for integrated circuits that have critical dimension smaller than 0.25 µm because of the "bird's beak" effect that allows the thermally grown silicon-dioxide region to encroach into the adjacent area where active circuit elements are to be built and the stress-induced silicon defects associated with the thermal process. The successor to LOCOS is shallow trench isolation (STI).

[0005] In STI a relatively shallow trench is first etched into the silicon substrate, which is then refilled with an insulator material. Following a short thermal-oxidation step that forms a thin film of SiO_2 on the trench walls and a refilling step that deposits a SiO_2 film on the chip, the surface is planarized by CMP to complete the isolation structure.

[0006] Since the bird's beak is entirely eliminated in a STI structure, smaller isolation spacing between circuit elements is possible compared with a LOCOS structure. In addition, the field oxide in STI is fully recessed, offering the potential of a completely planar surface after the isolation-structure formation.

[0007] STI significantly shrinks the area needed to isolate circuit elements and it provides better planarity. From a processing point of view, however, the formation of a STI structure that fully realizes the advantages is a little more complicated. One of the challenges lie in providing void-free, seamless gap-fill by CVD and uniform planarization by CMP; another in providing properly rounded corners at the upper edges of the trench. In the current art, void-avoidance is accomplished by the combination of using a high-density-plasma CVD (HDP-CVD) process, which includes sputter-etching action, and forming trenches with slanted sidewalls.

Brief Description of Drawings

[0008] Figure 1 depicts a unit cell of a diamond-structured crystal.

[0009] Figure 2 depicts a section of a silicon-crystal ingot and a (001) surface, and a enlargement of a silicon unit cell.

[0010] Figure 3 depicts a cross section of a partially processed silicon trench.

[0011] Figure 4 depicts a cross section of a further processed silicon trench.

[0012] Figure 5 depicts a cross section of a corner of a partially process silicon trench.

Description of the Preferred Embodiment

[0013] Before describing the invention, a brief description of the silicon crystal structure is in order.

[0014] As shown in Figure 1a, a silicon crystal is depicted in the form of its basic building block – a cubic unit cell that is approximately 5.43Å per side at room temperature. In the art of crystallography, the silicon crystal is referred to as having a 'diamond' lattice structure, the unit building block of which can be viewed as two interpenetrating face-centered cubic lattices which are simply cubic blocks with silicon atoms at each of the eight corners and at the center of each of the six sides.

[0015] Once the crystal structure is ascertained, information on the crystallographic facets can also be determined. For example, as shown in 1a, the top side of the unit cell passes through five silicon atoms – four at the four corners and one in the middle. Since each corner-atom is shared by four neighboring sides if the unit cell is repeated in the x, y, and z directions, the density of silicon atoms on the top plane is two atoms per side of the unit cell. Different planes in the crystal may have different density of silicon atoms.

[0016] Crystallographers use Miller indices to identify the various crystal-facets or crystallographic planes in a crystal. The Miller index of a crystal plane is defined by the distance and orientation of the plane relative to a set of orthogonal axes and the point of origin.

[0017] As shown in Figure 1b, for example the top side of the unit cell has a Miller index of (001) because it runs parallel to the x and y axes and it intersects the z axis at a distance 'a' from the origin where 'a' is the length of the side of the cubic unit cell. According to the art, all planes that runs parallel to this (001) plane and are distance 'a' from each other share the same Miller index (001). Planes that run parallel to the z and y axes and intersect the x-axis at integer intervals of 'a' are designated as the (100) planes and the plane that run parallel to the x and z axes and intersect the y-axis at intervals 'a' are designated as the (010) planes. And {100} designates a family of planes including the (100), (010), and (001) planes.

[0018] For the same token, a (100) plane defines a vector [100] that points perpendicularly away from the plane, and <100> designates a family of vectors including the [100], [010], and [001] vectors.

[0019] The following embodiment can be better explained with the aids of Miller indices. According to one embodiment of the invention, a STI structure may be formed as follows:

[0020] As shown in Figure 2, a pad-oxide layer 200 (about 100Å) is formed on a (100) silicon wafer 100. The silicon wafer may be of single crystalline silicon or it may be a pre-stressed silicon wafer with silicon-germanium layer near the top surface of the wafer. The pad oxide layer is formed to reduce stress that would exist if a silicon nitride layer 300 (which is deposited next) were deposited directly on the silicon-wafer. In a single crystalline silicon wafer, such stresses could cause defects. In a pre-stressed wafer, the additional stresses could also disturb the pre-determined strain built-in by the silicon-germanium layer.

[0021] Also as shown in Figure 2, a silicon-nitride layer 300 (about 1,200Å) is deposited on the pad-oxide layer. The nitride layer 300 serves two roles:

a. as a hard mask for etching the trench; and

b. as a polish-stop-layer when the trench-fill dielectric material is planarized with a CMP process.

[0022] Also as shown in Figure 2, photoresist 400 is applied and a STI mask is used to pattern the regions on the wafer surface where a STI trench will be formed. The trench-pattern puts the trench-edges along the <100> directions so that after trench etch. The significance of the orientation will be explained in a later paragraph.

[0023] As shown in Figure 3, the nitride 300 and pad-oxide 200 are anisotropically etched, in a plasma-etching apparatus.

[0024] Also as shown in Figure 3, the trench 10 is etched. This silicon-etch step is carried out in a plasma-etching apparatus using a mixture of HBr and other gases. The sidewalls 101 (as least the upper portion near the pad oxide) of the trench 10 are etched nearly vertically (within about 10 degrees) to the top surface of the silicon wafer. The

trench-etch process may be carried out in a second etcher, different from the one used to etch the nitride and oxide layers or it may be carried out in the same etcher. After the trench 10 is etched, the residual resist is stripped. Alternatively, the resist pattern 400 may be stripped from the top of the nitride layer 300 after the nitride-etch and before the silicon-etch process commences.

[0025] As shown in Figure 4, a controlled recess 201 in the pad oxide 200 underneath the nitride layer 300 is formed with a short HF dip prior to an oxidation step that forms the liner-oxide layer 202. The liner-oxide layer 202 passivates the silicon surface 101 of the trench to provide a stable interface between the silicon and the trench fill material. The liner-oxidation process also helps rounding the top corner of the trenches 10 as will be explained in the next paragraph.

[0026] As shown in Figure 3, the trench etching forms a sharp corner (between about 80 to 90 degrees) at the top of the trench. When a circuit element is built near such a sharp corner, the corner tends to enhance the local electric field. If the circuit element is a MOSFET, the locally enhanced electric field may cause undesirable effects, including degrading the transistor turn-off characteristics. Therefore, it is desirable that the top corner 102, as shown in Figure 4, be rounded.

[0027] Also as shown in Figure 5, the liner oxide 202 rounds the top corners 102 of the trench 10. The liner oxide 201 formed on the trench sidewalls 101 is 10-15-nm thick in this embodiment. The oxide at the upper corner 102 of the trench 10 should be about 1.5 times thicker to achieve good corner-rounding. Since the rate of oxide growth is a strong function of the orientation of the crystallographic surface exposing to the oxidation environment, the applicants recognize that one effective way to achieve desirable corner rounding is to form a trench of which the sidewalls near the upper corners are made of relatively slow-oxidizing crystallographic planes while faster oxidizing planes make up the corners. The applicants also recognize that among the major crystallographic planes, the {100} planes have the slowest rate of oxide growth. Major crystallographic planes mean those planes of which the Miller indices consist of low integer numbers such as 1, 2, or 3.

[0028] Therefore, it is desirable to pattern the trench with its edges align close to the <100> direction (to within 10 degrees) and etch the top portion of the trench anisotropically so that at least the sidewalls 101 near the upper corners are close to {100} planes. On the other hand, the crystallographic planes that make up the corners are necessarily faster oxidizing than the sidewalls. With such a configuration, the oxide film at the corners 102 is substantially thick than that at the sidewalls 101 and good corner rounding results.

[0029] The applicants also recognize that although the liner oxide may be formed by a rapid thermal oxidation (RTO) process, a furnace oxidation process in dry oxygen ambient with hydrogen chloride gas mixed therein produces a better oxide-to-silicon interface. The interface of a furnace-oxide, for example, has lower surface states density than the interface of RTO oxide.

[0030] In addition, for good oxide-thickness control, it is desirable to limit the oxidation-temperature to 900°C or below so that the total furnace process-time stays in a reasonable range of about 20 minutes. Higher oxidation temperature may be used but the control of the oxide thickness is superior at a temperature of 900°C or below.

[0031] One exemplary liner-oxidation process is as follows:

a. loading the wafer into the furnace at 700°C;

b. ramping the furnace temperature to 850°C;

c. providing a gaseous mixture of oxygen, trans-1,2 dichloethene (TRANS-LC® by SCHUMACHER) and nitrogen in the furnace while maintain the furnace-temperature at 850 °C for 25 minutes to grow a 80Å-layer of liner-oxide on a (100) silicon wafer surface;

d. ramping the furnace-temperature down to 700°C; and

e. unloading the wafer from the furnace at 700°C.

[0032] Inasmuch as the present invention is subject to variations, modifications and changes in detail it is intended that the subject matter discussed above and shown in the accompanying drawings be interpreted as illustrative and not in a limitation. For example, not all trenches in a integrated circuit chip need to be aligned to the same

direction if other design considerations so dictate; the liner-oxide-growth process temperature and the gaseous mixture may vary if the thickness of the liner oxide deviates from that in the embodiment. The invention may also be applied to wafers of other orientations than (100) and to semiconductor other than silicon as long as a differentiation in oxidation rate exists between the trench-corners and the sidewalls near the corners.